GL865/GL868 V3, GE866 Digital Voice Interface
Application Note
80000NT10104A Rev. 2 – 2014-04-16
APPLICABILITY TABLE

<table>
<thead>
<tr>
<th>GL Family (Embedded)</th>
<th>SW Versions</th>
</tr>
</thead>
<tbody>
<tr>
<td>GL865-DUAL V3</td>
<td>16.00.xx2</td>
</tr>
<tr>
<td>GL866-QUAD V3</td>
<td>16.00.xx3</td>
</tr>
</tbody>
</table>

Note: the features described in the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table. See also the Document History chapter.
Notice
While reasonable efforts have been made to assure the accuracy of this document, Telit assumes no liability resulting from any inaccuracies or omissions in this document, or from use of the information obtained herein. The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies or omissions. Telit reserves the right to make changes to any products described herein and reserves the right to revise this document and to make changes from time to time in content hereof with no obligation to notify any person of revisions or changes. Telit does not assume any liability arising out of the application or use of any product, software, or circuit described herein; neither does it convey license under its patent rights or the rights of others.

It is possible that this publication may contain references to, or information about Telit products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that Telit intends to announce such Telit products, programming, or services in your country.

Copyrights
This instruction manual and the Telit products described in this instruction manual may be, include or describe copyrighted Telit material, such as computer programs stored in semiconductor memories or other media. Laws in the Italy and other countries preserve for Telit and its licensors certain exclusive rights for copyrighted material, including the exclusive right to copy, reproduce in any form, distribute and make derivative works of the copyrighted material. Accordingly, any copyrighted material of Telit and its licensors contained herein or in the Telit products described in this instruction manual may not be copied, reproduced, distributed, merged or modified in any manner without the express written permission of Telit. Furthermore, the purchase of Telit products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Telit, as arises by operation of law in the sale of a product.

Computer Software Copyrights
The Telit and 3rd Party supplied Software (SW) products described in this instruction manual may include copyrighted Telit and other 3rd Party supplied computer programs stored in semiconductor memories or other media. Laws in the Italy and other countries preserve for Telit and other 3rd Party supplied SW certain exclusive rights for copyrighted computer programs, including the exclusive right to copy or reproduce in any form the copyrighted computer program. Accordingly, any copyrighted Telit or other 3rd Party supplied SW computer programs contained in the Telit products described in this instruction manual may not be copied (reverse engineered) or reproduced in any manner without the express written permission of Telit or the 3rd Party SW supplier. Furthermore, the purchase of Telit products shall not be deemed to grant either directly or by implication, estoppel, or otherwise, any license under the copyrights, patents or patent applications of Telit or other 3rd Party supplied SW, except for the normal non-exclusive, royalty free license to use that arises by operation of law in the sale of a product.
USAGE AND DISCLOSURE RESTRICTIONS

License Agreements
The software described in this document is the property of Telit and its licensors. It is furnished by express license agreement only and may be used only in accordance with the terms of such an agreement.

Copyrighted Materials
Software and documentation are copyrighted materials. Making unauthorized copies is prohibited by law. No part of the software or documentation may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means, without prior written permission of Telit.

High Risk Materials
Components, units, or third-party products used in the product described herein are NOT fault-tolerant and are NOT designed, manufactured, or intended for use as on-line control equipment in the following hazardous environments requiring fail-safe controls: the operation of Nuclear Facilities, Aircraft Navigation or Aircraft Communication Systems, Air Traffic Control, Life Support, or Weapons Systems (High Risk Activities”). Telit and its supplier(s) specifically disclaim any expressed or implied warranty of fitness for such High Risk Activities.

Trademarks
TELI.T and the Stylized T Logo are registered in Trademark Office. All other product or service names are the property of their respective owners.

Copyright © Telit Communications S.p.A.
Contents

1. Introduction .......................................................................................................................... 7
   1.1. Scope .............................................................................................................................. 7
   1.2. Audience ......................................................................................................................... 7
   1.3. Contact Information, Support ...................................................................................... 7
   1.4. Related Documents ....................................................................................................... 8
   1.5. Document History ......................................................................................................... 8
   1.6. Abbreviations and Acronyms ....................................................................................... 8

2. DVI Overview ......................................................................................................................... 9

3. DVI Bus .................................................................................................................................. 10

4. DVI AT Commands .............................................................................................................. 11
   4.1. AT#DVI ......................................................................................................................... 11
   4.2. AT#DVIEXT .................................................................................................................. 12

5. DVI Setting Examples .......................................................................................................... 13
   5.1. Normal (I'S) Mode ....................................................................................................... 14
       5.1.1. Module is Master .................................................................................................. 14
       5.1.2. Module is Slave .................................................................................................... 17
   5.2. Burst Mode (PCM) ...................................................................................................... 19
       5.2.1. Module is Master .................................................................................................. 19
       5.2.2. Module is Slave .................................................................................................... 22

6. Annex .................................................................................................................................... 25
   6.1. I'S Bus Overview ......................................................................................................... 25
   6.2. Schematic ...................................................................................................................... 26
Figures

fig. 1: Example of Digital Voice Interface Use..............................................................9
fig. 2: Master and Slave Configurations.........................................................................10
fig. 3: Telit Module/Codec Connections.........................................................................13
fig. 4: DVI Configurations.............................................................................................13
fig. 5: Module is Master/Normal mode/ N bits per sample/Dual Mono.........................14
fig. 6: Module is Master/Normal mode/16 bits per sample/Dual Mono/<edge>=0........16
fig. 7: Module is Slave/Normal mode/24 bits per sample/Dual Mono/<edge>=0...........18
fig. 8: Module is Master/Burst mode/N bits per sample/Mono Mode............................19
fig. 9: Module is Master/Burst Mode/16 bits per Sample/Mono Mode/<edge>=1...........21
fig. 10: Module is Slave/Burst mode/N bits per sample/Mono Mode..............................22
fig. 11: Module is Slave/Burst mode/16 bits per sample/Mono Mode/<edge>=1............24
fig. 12: I2S Bus Configurations......................................................................................25
fig. 13: Schematic for Reference Design.........................................................................26

Tables

Tab. 1: DVI Signals...........................................................................................................10
Tab. 2: DVI configuration via AT#DVI command..............................................................11
Tab. 3: DVI Audio Format configuration via AT#DVIEXT command..........................12
Tab. 4: BitClockFrequency generated by the module in Master/Normal Mode..............14
Tab. 5: BitClockFrequency generated by the module in Master/Burst Mode...............19
1. **Introduction**

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit’s modules shown in the Applicability Table.

1.1. **Scope**

This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows some configurations of a popular Audio Codec connected to the module. These activities are accomplished via I²S and I²C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2. **Audience**

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. **Contact Information, Support**

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

- TS-EMEA@telit.com
- TS-NORTHAMERICA@telit.com
- TS-LATINAMERICA@telit.com
- TS-APAC@telit.com

Alternatively, use:


For detailed information about where you can buy the Telit Modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC). Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements. Telit appreciates feedback from the users of our information.
1.4. Related Documents


1.5. Document History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Products / SW Versions</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2013-09-09</td>
<td>/</td>
<td>First issue</td>
</tr>
<tr>
<td>1</td>
<td>2014-03-06</td>
<td>/</td>
<td>Chapter 4: Added the sentence: “The Digital Voice Interface supports the Echo canceller functionality, refer to document [3] for the specific AT commands”</td>
</tr>
<tr>
<td>2</td>
<td>2014-04-16</td>
<td>/</td>
<td>The document title has been changed from “GL865/GL868 V3 Digital Voice Interface” into “GL865/GL868 V3, GE866 Digital Voice Interface”. The note about the Echo canceller has been moved into chapter 2. The chapters numbering/naming has been reorganized.</td>
</tr>
</tbody>
</table>

Products added:
GE866-QUAD/16.00.xx3

1.6. Abbreviations and Acronyms

- DTE  Data Terminal Equipment
- DVI  Digital Voice Interface
- GPIO General Purpose Input/Output
- I2C  Inter-Integrated Circuit
- I2S  Inter-IC Sound
- MSB  Most Significant Bit
2. **DVI Overview**

Before dealing with the configuration and technical aspects of the Telit’s Digital Voice Interface (DVI) it is useful to illustrate briefly how this interface can be used, refer to fig. 1.

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit’s module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.

![DVI Diagram](image)

**fig. 1: Example of Digital Voice Interface Use**

**NOTICE:** the Digital Voice Interface supports the Echo canceller functionality, which is beyond the scope of the present document. Refer to document [3] for the specific AT commands.
3. DVI Bus

The physical DVI interface provided by the modules of the Telit’s GL family is based on the standard I²S Bus. An overview of the standard I²S Bus is described in chapter 6.1. Tab. 1 summarizes the DVI signals and a short description for each one of them; refer to documents [1], [4], or [5] to have information on electrical characteristics and signals pin-out.

<table>
<thead>
<tr>
<th>DVI Signal</th>
<th>DVI Signal name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>DVI_CLK</td>
<td>Data Clock</td>
</tr>
<tr>
<td>Word Alignment</td>
<td>DVI_WAO</td>
<td>Frame Synchronism</td>
</tr>
<tr>
<td>serial audio data input</td>
<td>DVI_RX</td>
<td>Received Data</td>
</tr>
<tr>
<td>serial audio data output</td>
<td>DVI_TX</td>
<td>Transmitted Data</td>
</tr>
</tbody>
</table>

Tab. 1: DVI Signals

The figures below show the two configurations of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself, otherwise, when it is Slave, both signals are generated by the connected Audio Device Codec.

In general, before establishing a voice call it is possible to select one of the two configurations and in accordance with the selected setting, configure the module and the codec via the AT commands provided by Telit [3]. The next pages describe the use of these AT commands.

fig. 2: Master and Slave Configurations
4. DVI AT Commands

Several DVI audio bus configurations are available via AT#DVI and AT#DVIEXT commands. The tables in the following sub-sections summarize their parameters; refer to document [3] for AT commands syntax details.

4.1. AT#DVI

AT#DVI command enables/disables the DVI interface, selects the DVI port, and sets the module in Master or Slave configuration.

The following table shows the AT command parameters values.

<table>
<thead>
<tr>
<th>AT#DVI =&lt;mode&gt;,&lt;dviport&gt;,&lt;clockmode&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;mode&gt;</td>
</tr>
<tr>
<td>0 -&gt; disable DVI interface</td>
</tr>
<tr>
<td>1 -&gt; enable DVI interface</td>
</tr>
<tr>
<td>2 -&gt; reserved</td>
</tr>
<tr>
<td>&lt;dviport&gt;</td>
</tr>
<tr>
<td>1 -&gt; select DVI port 1, factory setting</td>
</tr>
<tr>
<td>2 -&gt; reserved</td>
</tr>
<tr>
<td>&lt;clockmode&gt;</td>
</tr>
<tr>
<td>0 -&gt; DVI slave</td>
</tr>
<tr>
<td>1 -&gt; DVI master, factory setting</td>
</tr>
</tbody>
</table>

Tab. 2: DVI configuration via AT#DVI command
4.2. AT#DVIEXT

AT#DVIEXT command sets the module in Normal or Burst DVI Audio Format:

- In Normal DVI Audio Format the WAO signal defines the left and right audio channel.
- In Burst DVI Audio Format the WAO signal defines the beginning of the audio frame.

The following table shows the AT command parameters values.

<table>
<thead>
<tr>
<th>DVI Audio Format [Mode]</th>
<th>AT#DVIEXT (&lt;config&gt;,&lt;samplerate&gt;,&lt;samplewidth&gt;,&lt;audiomode&gt;,&lt;edge&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(&lt;config&gt;) (&lt;samplerate&gt;) (&lt;samplewidth&gt;) (&lt;audiomode&gt;) (&lt;edge&gt;)</td>
</tr>
<tr>
<td>Normal [I²S]</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>(0 \rightarrow 8 \text{ [KHz]} \text{ sample rate})</td>
</tr>
<tr>
<td></td>
<td>(1 \rightarrow \text{ reserved})</td>
</tr>
<tr>
<td></td>
<td>(16 \text{ bits per sample})</td>
</tr>
<tr>
<td></td>
<td>(2 \rightarrow \text{ reserved})</td>
</tr>
<tr>
<td></td>
<td>(24 \text{ bits per sample})</td>
</tr>
<tr>
<td></td>
<td>(32 \text{ bits per sample})</td>
</tr>
<tr>
<td>Burst [PCM]</td>
<td>0 \text{ factory setting})</td>
</tr>
<tr>
<td></td>
<td>(1 \rightarrow \text{ reserved})</td>
</tr>
<tr>
<td></td>
<td>(\text{the rising edge of})</td>
</tr>
<tr>
<td></td>
<td>(\text{the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock.})</td>
</tr>
<tr>
<td></td>
<td>(0 \rightarrow \text{ has the same behavior of 1})</td>
</tr>
</tbody>
</table>

Tab. 3: DVI Audio Format configuration via AT#DVIEXT command
5. **DVI Setting Examples**

The next chapters show examples concerning the audio formats supported by the DVI audio bus in Master and Slave configurations. All the following setting examples are performed using the hardware configuration shown in fig. 3. I²C bus is used to configure the MAX9867 Codec\(^1\) [2]: the user by means of AT commands can control the codec. The DVI bus provides the voice connection between the two devices.

The setting examples are organized as shown in the figure below.

![Diagram](image)

fig. 3: Telit Module/Codec Connections

![Diagram](image)

fig. 4: DVI Configurations

---

\(^1\) The following examples use the MAX9867 Codec, see chapter 6.2 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the used module.
5.1. Normal (I²S) Mode

5.1.1. Module is Master

The fig. 5 shows a timing diagram that refers to the module in the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the two audio channels: left and right.

![Timing Diagram](image)

fig. 5: Module is Master/Normal mode/ N bits per sample/Dual Mono

When module is Master the BitClockFrequency (CLK) is provided by the following expression:

\[
\text{BitClockFrequency} = \text{DataWordBit} \times \text{ChannelNumber} \times \text{AudioSampleRate}
\]

Refer to Tab. 4 for the BitClockFrequency generated by the module.

<table>
<thead>
<tr>
<th>&lt;samplewidth&gt;</th>
<th>DataWordBit</th>
<th>Audio channels</th>
<th>AudioSampleRate: 8 KHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>16</td>
<td>2</td>
<td>256</td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>24</td>
<td>2</td>
<td>384</td>
</tr>
<tr>
<td>4</td>
<td>32</td>
<td>2</td>
<td>512</td>
</tr>
</tbody>
</table>

Tab. 4: BitClockFrequency generated by the module in Master/Normal Mode
Here are the lists of AT commands used to set the module in Master Normal (I²S) Mode, and configure the codec in accordance with the module setting. After each command is described the used parameters values meaning.

### Configure the module in Master Normal (I²S) Mode

**AT#DVI=1,1,1**

**OK**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>enable DVI interface</td>
</tr>
<tr>
<td>1</td>
<td>use DVI port 1 (mandatory)</td>
</tr>
<tr>
<td>1</td>
<td>set the module as Master (factory setting)</td>
</tr>
</tbody>
</table>

**AT#DVIEXT=1,0,0,1,0**

**OK**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Normal Mode</td>
</tr>
<tr>
<td>0</td>
<td>sample rate 8 KHz (mandatory)</td>
</tr>
<tr>
<td>0</td>
<td>16 bits per sample</td>
</tr>
<tr>
<td>1</td>
<td>Dual Mono, the same Data Word is transmitted on both audio channels</td>
</tr>
<tr>
<td>0</td>
<td>data is transmitted on falling edge of clock and sampled on rising edge of clock</td>
</tr>
</tbody>
</table>

### Configure the codec in Slave Normal (I²S) Mode

**AT#I2CWR=X,Y,30,4,19**

>`00109000100A330000330C0C0902424400060`

**OK**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>GPIO number used as SDA, refer to [3]</td>
</tr>
<tr>
<td>Y</td>
<td>GPIO number used as SCL, refer to [3]</td>
</tr>
<tr>
<td>30</td>
<td>Device address on I²C, refer to [2]</td>
</tr>
<tr>
<td>4</td>
<td>Register address from which start the writing, refer to [2]</td>
</tr>
<tr>
<td>19</td>
<td>number of bytes to write</td>
</tr>
<tr>
<td>&gt;00109000…..</td>
<td>refer to [2]</td>
</tr>
</tbody>
</table>

**AT#I2CWR=X,Y,30,17,1**

>`8A`

**OK**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>GPIO number used as SDA, refer to [3]</td>
</tr>
<tr>
<td>Y</td>
<td>GPIO number used as SCL, refer to [3]</td>
</tr>
<tr>
<td>30</td>
<td>Device address on I²C, refer to [2]</td>
</tr>
<tr>
<td>17</td>
<td>Register address where write data, refer to [2]</td>
</tr>
<tr>
<td>1</td>
<td>number of bytes to write</td>
</tr>
<tr>
<td>&gt;8A</td>
<td>refer to [2]</td>
</tr>
</tbody>
</table>
The fig. 6 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (256 KHz) and WAO signals are generated by the module.

Left channel:

\[ \downarrow \]: Data transitions occur on the falling edge of the CLK

\[ \uparrow \]: Data are latched on the rising edge of the CLK

Right channel:

\[ \downarrow \]: Data transitions occur on the falling edge of the CLK

\[ \uparrow \]: Data are latched on the rising edge of the CLK

fig. 6: Module is Master/Normal mode/16 bits per sample/Dual Mono/<edge>=0
5.1.2. Module is Slave

Here are the lists of the AT commands used to set the module in Slave Normal (I²S) Mode, and configure the Codec in accordance with the module setting. After each command is described the used parameters values meaning.

Configure the Module in Slave-Normal (I²S) Mode

AT#DVI=1,1,0
OK

1 enable DVI interface
1 use DVI port 1 (mandatory)
0 set the module as Slave

AT#DVIEXT=1,0,3,1,0
OK

1 Normal Mode
0 sample rate 8 KHz (mandatory)
3 24 bits per sample
1 Dual Mono, the same Data Word is transmitted on both audio channels
0 data is transmitted on falling edge of clock and sampled on rising edge of clock

Configure the Codec in Master-Normal (I²S) Mode

AT#I2CWR=X,Y,30,4,19
>00101000900233000330C09092424400060
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I2C
4 Register address from which start the writing
19 number of bytes to write
>00101000…….refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I2C
17 Register address where write data
1 number of bytes to write
>8A refer to [2]

NOTICE: the Codec is in Master configuration and generates a clock equal to 384 KHz. On the module the selected number of bits per sample is 24, see Tab. 4

The fig. 7 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec.
Left channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

Right channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

fig. 7: Module is Slave/Normal mode/24 bits per sample/Dual Mono/<edge>=0
5.2. Burst Mode (PCM)

5.2.1. Module is Master

The fig. 8 shows a timing diagram that refers to the module in the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the audio channel.

![Diagram](image)

**fig. 8: Module is Master/Burst mode/N bits per sample/Mono Mode**

When module is Master the BitClockFrequency (CLK) is provided by the following expression:

\[
\text{BitClockFrequency} = (\text{DataWordBit} + 1) \times \text{AudioSampleRate}
\]

Refer to Tab. 5 for the BitClockFrequency generated by the Module.

<table>
<thead>
<tr>
<th>samplewidth</th>
<th>DataWordBit</th>
<th>Audio channels</th>
<th>AudioSampleRate: 8 KHz BitClockFrequency in KHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>16 [+ 1]</td>
<td>1</td>
<td>136</td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>reserved</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>32 [+ 1]</td>
<td>1</td>
<td>264</td>
</tr>
</tbody>
</table>

**Tab. 5: BitClockFrequency generated by the module in Master/Burst Mode**

2 The width of the WAO pulse is 1 CLK.
Below is the list of the AT commands used to set the module in Master Burst (PCM) Mode, and configure the codec in accordance with the current module setting.

**Configure the module in Master-Burst (PCM) Mode**

```plaintext
AT#DVI=1,1,1
OK

1 enable DVI interface
1 use DVI port 1 (mandatory)
1 set the module DVI as Master (factory setting)

AT#DVIEXT=0,0,0,0,1
OK

0 Burst Mode (PCM) (factory setting)
0 sample rate 8 KHz (mandatory)
0 16 bits per sample
0 Mono Mode
1 the rising edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock (0 has the same behavior).
```

**Configure the codec in Slave Burst (PCM) Mode.**

```plaintext
AT#I2CWR=X,Y,30,4,19
> 00109000600A33000033C0C09092424400060
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I2C
4 Register address from which start the writing
19 number of bytes to write
>00109000.....refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I2C
17 Register address where write data
1 number of bytes to write
>8A refer to [2]
```
The fig. 9 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (136 KHz) and WAO signals are generated by the module.

↑: Data transitions occur on the rising edge of the CLK
↓: Data are latched on the falling edge of the CLK

fig. 9: Module is Master/Burst Mode/16 bits per Sample/Mono Mode/<edge>=1
5.2.2. Module is Slave

The fig. 10 shows a timing diagram that refers to the codec in master configuration. In this case, the WAO and CLK signals are generated by the codec.

fig. 10: Module is Slave/Burst mode/N bits per sample/Mono Mode
Here are the lists of AT commands used to set the module in Slave Burst (PCM) Mode, and configure the Codec in accordance with the current module setting. After each command is described the used parameters values meaning.

### Configure the module in Slave Burst (PCM) Mode.

<table>
<thead>
<tr>
<th>Command</th>
<th>Parameters</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>AT#DVI=1,1,0</code></td>
<td>OK</td>
<td>enable DVI interface&lt;br&gt;1 use DVI port 1 (mandatory)&lt;br&gt;0 set the module as Slave</td>
</tr>
<tr>
<td><code>AT#DVIEXT=0,0,0,1</code></td>
<td>OK</td>
<td>0 Burst Mode (factory setting)&lt;br&gt;0 sample rate 8 KHz (mandatory)&lt;br&gt;0 16 bits per sample&lt;br&gt;0 Mono Mode&lt;br&gt;1 the rising edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock (0 has the same behavior).</td>
</tr>
</tbody>
</table>

### Configure the Codec in Master Burst PCM Mode.

<table>
<thead>
<tr>
<th>Command</th>
<th>Parameters</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>AT#I2CWR=X,Y,30,4,19</code></td>
<td>OK</td>
<td>00101000 A4 0A 33 0000 310C0C 09 09 24 24 40 00 60&lt;br&gt;X GPIO number used as SDA&lt;br&gt;Y GPIO number used as SCL&lt;br&gt;30 Device address on I²C&lt;br&gt;4 Register address from which start the writing&lt;br&gt;19 number of bytes to write&lt;br&gt;&amp;00101000.....refer to [2]</td>
</tr>
<tr>
<td><code>AT#I2CWR=X,Y,30,17,1</code></td>
<td>OK</td>
<td>8A&lt;br&gt;X GPIO number used as SDA&lt;br&gt;Y GPIO number used as SCL&lt;br&gt;30 Device address on I²C&lt;br&gt;17 Register address where write data&lt;br&gt;1 number of bytes to write&lt;br&gt;&amp;8A refer to [2]</td>
</tr>
</tbody>
</table>
The fig. 11 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec.

↑: Data transitions occur on the rising edge of the CLK
↓: Data are latched on the falling edge of the CLK

![Timing Diagram](image.png)

Audio sample rate: 8 KHz

16 bits per sample
32 bits do not used

fig. 11: Module is Slave/Burst mode/16 bits per sample/Mono Mode/edge>=1
6. Annex

6.1. I²S Bus Overview

This chapter provides a short description of the standard I²S bus. This standard suitably modified is used by the DVI interface implemented on the Telit modules.

The standard I²S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to fig. 12: the I²S design handles audio data separately from clock signals. On an I²S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I²S bus clock.

An I²S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I²S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

![I²S Bus Configurations](image-url)

fig. 12: I²S Bus Configurations
6.2. Schematic

A schematic example of an interface between a Telit Module and the MAX9867 Codec could be the following:

![Schematic Diagram]

fig. 13: Schematic for Reference Design