**APPLICABILITY TABLE**

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**Note:** the features described in the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table. See also the Document History chapter.
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1. **Introduction**

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit’s modules shown in the Applicability Table.

1.1. **Scope**

This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows some configurations of a popular Audio Codec connected to the module. These activities are accomplished via I2S and I2C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2. **Audience**

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. **Contact Information, Support**

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

- TS-EMEA@telit.com
- TS-NORTHAMERICA@telit.com
- TS-LATINAMERICA@telit.com
- TS-APAC@telit.com

Alternatively, use:


For detailed information about where you can buy the Telit Modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.
1.4. **Related Documents**

[1] MAX9867 Ultra-Low Power Stereo Audio Codec, MAXIM

1.5. **Document History**

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1.6. **Abbreviations and Acronyms**

- **DTE**: Data Terminal Equipment
- **DVI**: Digital Voice Interface
- **GPIO**: General Purpose Input/Output
- **I2C**: Inter-Integrated Circuit
- **I2S**: Inter-IC Sound
- **MSB**: Most Significant Bit
2. DVI Overview

Before dealing with the configuration and technical aspects of the Telit’s Digital Voice Interface (DVI) it is useful to illustrate briefly how this interface can be used, refer to fig. 1.

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit’s module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.

fig. 1: Example of Digital Voice Interface Use

**NOTICE:** the Digital Voice Interface supports the Echo canceller functionality, which is beyond the scope of the present document. Refer to document [2] for the specific AT commands.
3. DVI Bus

The physical DVI interface provided by the Telit’s modules is based on the standard I2S Bus. An overview of the standard I2S Bus is described in chapter 6.1. Tab. 1 summarizes the DVI signals and a short description for each one of them; refer to Telit Hardware User Guide, in accordance with the used module, to have information on electrical characteristics, number of DVI ports, and signals pin-out.

<table>
<thead>
<tr>
<th>DVI Signal</th>
<th>DVI Signal name</th>
<th>Description</th>
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<tbody>
<tr>
<td>Clock</td>
<td>DVI_CLK</td>
<td>Data Clock</td>
</tr>
<tr>
<td>Word Alignment</td>
<td>DVI_WAO</td>
<td>Frame Synchronism</td>
</tr>
<tr>
<td>serial audio data input</td>
<td>DVI_RX</td>
<td>Received Data</td>
</tr>
<tr>
<td>serial audio data output</td>
<td>DVI_TX</td>
<td>Transmitted Data</td>
</tr>
</tbody>
</table>

Tab. 1: DVI Signals

The figures below show the two configurations of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself, otherwise, when it is Slave, both signals are generated by the connected Audio Device Codec.

In general, before establishing a voice call it is possible to select one of the two configurations and in accordance with the selected setting, configure the module and the codec via the AT commands provided by document [2]. The next pages describe the use of these AT commands.

![fig. 2: Master and Slave Configurations](image-url)
4. **DVI AT Commands**

Several DVI audio bus configurations are available via AT#DVI and AT#DVIEXT commands. The tables in the following sub-sections summarize their parameters; refer to document [2] for AT commands syntax details.

4.1. **AT#DVI**

AT#DVI command enables/disables the DVI interface, selects the DVI port, and sets the module in Master or Slave configuration. The table below shows the AT command parameters values.

<table>
<thead>
<tr>
<th>&lt;mode&gt;</th>
<th>&lt;dviport&gt;</th>
<th>&lt;clockmode&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>disable DVI interface</td>
<td>0 → DVI slave</td>
</tr>
<tr>
<td>1</td>
<td>enable DVI interface</td>
<td>1 → DVI master, factory setting</td>
</tr>
<tr>
<td>2</td>
<td>enable DVI interface and analog lines</td>
<td></td>
</tr>
</tbody>
</table>

1 → select DVI port 1, factory setting
2 → select DVI port 2, refer to the Hardware User Guide of the used module to know if it supports the DVI port 2

Tab. 2: DVI configuration via AT#DVI command
4.2. **AT#DVIEXT**

AT#DVIEXT command sets the module in Normal or Burst DVI Audio Format:

- In Normal DVI Audio Format the WAO signal defines the left and right audio channel.
- In Burst DVI Audio Format the WAO signal defines the beginning of the audio frame.

The following table shows the AT command parameters values.

<table>
<thead>
<tr>
<th>DVI Audio Format (Mode)</th>
<th>AT#DVIEXT &lt;config&gt;,&lt;samplerate&gt;,&lt;samplewidth&gt;,&lt;audiomode&gt;,&lt;edge&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt;config&gt;</td>
</tr>
<tr>
<td>Normal (I2S)</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Burst (PCM)</td>
<td>0 factory setting</td>
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</table>

Tab. 3: DVI Audio Format configuration via AT#DVIEXT command
5. **DVI Setting Examples**

The next chapters show examples concerning the audio formats supported by the DVI audio bus in Master and Slave configurations. All the following setting examples are performed using the hardware configuration shown in fig. 3. I²C bus is used to configure the MAX9867 Codec\(^1\) [1]: the user by means of AT commands can control the codec. The DVI bus provides the voice connection between the two devices.

![fig. 3: Telit Module/Codec Connections](image)

The setting examples are organized as shown in the figure below.

![fig. 4: DVI Configurations](image)

---

\(^1\)The following examples use the MAX9867 Codec, see chapter 6.2 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the used module.
5.1. Normal (I²S) Mode

5.1.1. Module is Master

In this configuration the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the two audio channels: left and right, refer to fig. 5. The BitClockFrequency (CLK) is provided by the following expression:

\[ \text{BitClockFrequency} = \text{DataWordBit} \times \text{ChannelNumber} \times \text{AudioSampleRate} \]

The BitClockFrequency values are shown in Tab. 4.

<table>
<thead>
<tr>
<th>samplewidth</th>
<th>DataWordBit</th>
<th>Audio channels</th>
<th>AudioSampleRate: 8 KHz</th>
<th>BitClockFrequency in KHz</th>
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</thead>
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<td>0</td>
<td>16</td>
<td>2</td>
<td>256</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>3</td>
<td>24</td>
<td>2</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>32</td>
<td>2</td>
<td>reserved</td>
<td></td>
</tr>
</tbody>
</table>

Tab. 4: BitClockFrequency generated by the module in Master/Normal Mode

Here are the lists of AT commands used to set the module in Master/Normal (I²S) Mode, and configure the codec in accordance with the module setting. The meanings of the used parameters values are described after each command.
Configure the module in Master/Normal (I²S) Mode

**AT#DVI=1,1,1**

**OK**

- 1 enable DVI interface
- 1 use DVI port 1
- 1 set the module as Master (factory setting)

Setting for BitClockFrequency = 256 KHz

**AT#DVIEXT=1,0,0,1,1**

**OK**

- 1 Normal Mode
- 0 sample rate 8 KHz (mandatory)
- 0 16 bits per sample
- 1 Dual Mono, the same Data Word is transmitted on both audio channels
- 1 data is transmitted on the rising edge of clock and sampled on the falling edge

Setting for BitClockFrequency = 512 KHz

**AT#DVIEXT=1,0,4,1,1**

**OK**

- 1 Normal Mode
- 0 sample rate 8 KHz (mandatory)
- 4 32 bits per sample
- 1 Dual Mono, the same Data Word is transmitted on both audio channels
- 1 data is transmitted on the rising edge of clock and sampled on the falling edge
Configure the codec in Slave/Normal (I²S) Mode

AT#I2CWR=X,Y,30,4,19
>00109000200A330000330C0C09092424400060
OK

X  GPIO number used as SDA, refer to [2]
Y  GPIO number used as SCL, refer to [2]
30 Device address on I²C, refer to [1]
4  Register address from which start the writing, refer to [1]
19 number of bytes to write
>00109000…..refer to [1]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X  GPIO number used as SDA, refer to [2]
Y  GPIO number used as SCL, refer to [2]
30 Device address on I²C, refer to [1]
17 Register address where write data, refer to [1]
1  number of bytes to write
>8A refer to [1]
The fig. 5 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (256 KHz) and WAO signals are generated by the module, data is transmitted on the rising edge of clock and sampled on the falling edge.

**Left channel:**

↑: Data transitions occur on the rising edge of the CLK

↓: Data are latched on the falling edge of the CLK

**Right channel:**

↑: Data transitions occur on the rising edge of the CLK

↓: Data are latched on the falling edge of the CLK

fig. 5: Module is Master/Normal mode/16 bits per sample/Dual Mono/edge = 1
5.1.2.  Module is Slave

Below are the lists of the AT commands used to set the module in Slave/Normal (I²S) Mode, and configure the codec in accordance with the module setting. The meanings of the used parameters values are described after each command.

### Configure the Module in Slave/Normal (I²S) Mode

**AT#DVI=1,1,0**

OK

1  enable DVI interface
1  use DVI port 1
0  set the module as Slave

**AT#DVIEXT=1,0,3,1,0**

OK

1  Normal Mode
0  sample rate 8 KHz (mandatory)
3  24 bits per sample
1  Dual Mono, the same Data Word is transmitted on both audio channels
0  data is transmitted on the falling edge of the clock and sampled on the rising edge

### Configure the Codec in Master/Normal (I²S) Mode

**AT#I2CWR=X,Y,30,4,19**

>001010008002330000330C0C09092424400060

OK

X  GPIO number used as SDA
Y  GPIO number used as SCL
30  Device address on I2C
4  Register address from which start the writing
19  number of bytes to write
>00101000…..refer to [1]

**AT#I2CWR=X,Y,30,17,1**

>8A

OK

X  GPIO number used as SDA
Y  GPIO number used as SCL
30  Device address on I2C
17  Register address where write data
1  number of bytes to write
>8A  refer to [1]

**NOTICE:** the Codec is in Master configuration and generates a clock equal to 384 KHz. On the module the selected number of bits per sample is 24, see Tab. 4
The fig. 6 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec, data is transmitted on the falling edge of the clock and sampled on the rising edge.

Left channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

Right channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

![Timing Diagram](image)

fig. 6: Module is Slave/Normal mode/24 bits per sample/Dual Mono/ `<edge>` = 0
5.2. Burst Mode (PCM)

5.2.1. Module is Master

This configuration is not available yet.

5.2.2. Module is Slave

The fig. 7 shows a timing diagram that refers to the codec in master configuration. In this case, the WAO and CLK signals are generated by the codec.

![Timing Diagram](image)

fig. 7: Module is Slave/Burst mode/N bits per sample/Mono Mode

<table>
<thead>
<tr>
<th>DataWordBit</th>
<th>Bits discarded</th>
<th>AudioSampleRate: 8 KHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

BitClockFrequency in KHz

(DataWordBit + Bits discarded) x 8KHz = 384KHz

Tab. 5: BitClockFrequency generated by the codec in Master/Burst Mode (PCM)
Here are the lists of AT commands used to set the module in Slave/Burst (PCM) Mode, and configure the codec in accordance with the module setting. The meanings of the used parameters values are described after each command.

Configure the module in Slave/Burst (PCM) Mode.

```
AT#DVI=1,1,0
OK

1  enable DVI interface
1  use DVI port 1
0  set the module as Slave
```

```
AT#DVIEXT=0,0,0,1
OK

0  Burst Mode
0  sample rate 8 KHz (mandatory)
0  16 bits per sample
0  fixed value
1/0  data is transmitted on the rising edge of the clock and sampled on the falling edge
```

Configure the Codec in Master/Burst (PCM) Mode.

```
AT#I2CWR=X,Y,30,4,19
> 00101000A40A330000330C0C09092424400060
OK

X  GPIO number used as SDA
Y  GPIO number used as SCL
30  Device address on I2C
4  Register address from which start the writing
19  number of bytes to write
>00101000.....refer to [1]
```

```
AT#I2CWR=X,Y,30,17,1
>8A
OK

X  GPIO number used as SDA
Y  GPIO number used as SCL
30  Device address on I2C
17  Register address where write data
1  number of bytes to write
>8A  refer to [1]
```
The fig. 8 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec, data is transmitted on the rising edge of clock and sampled on the falling edge.

\[\uparrow\] Data transitions occur on the rising edge of the CLK

\[\downarrow\] Data are latched on the falling edge of the CLK

Audio sample rate: 8 MHz

16 bits per sample

32 bits do not

WAO generated by Codec

CLK generated by Codec

Module Tx / Codec Rx

Codec Tx / Module Rx

fig. 8: Module is Slave/Burst mode/16 bits per sample/Mono Mode
6. Annex

6.1. I²S Bus Overview

This chapter provides a short description of the standard I²S bus. This standard suitably modified is used by the DVI interface implemented on the Telit modules.

The standard I²S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to fig. 9: the I²S design handles audio data separately from clock signals. On an I²S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I²S bus clock.

An I²S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I²S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

![I²S Bus Configurations](image)

fig. 9: I²S Bus Configurations
6.2. Schematic

A schematic example of an interface between a Telit Module and the MAX9867 Codec could be the following:

![Schematic Diagram]

fig. 10: Schematic for Reference Design