Digital Voice Interface Application Note

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APPLICABILITY TABLE

This documentation applies to the following product families:

Table 1: Applicability Table

Module Name	Description
LE910-EU	
LE910-NA	
LE910-NV	
LE920-EU	
LE920-NA	
LE920-CN	
LE920A4-EU	
LE920A4-NA	
LE920A4-CN	
LE940A6-NA	
LE940A9-CN	
LE910C1-NA	North America – AT&T with global roaming
LE910C1-NS	North America - Sprint variant
LE910C1-AP	APAC variant CAT1 variant
LE910C4-AP	APAC variant CAT4 variant
LE910C4-EU	Europe CAT4 variant
LE910C1-EU	Europe CAT1 variant
LE910C1-EUX	Europe CAT1 variant
LE910C4-NF	North America CAT4 variant
LE910C1-NF	North America CAT1 variant
LE910C1-SA	North America CAT1 variant – AT&T
LE910C1-SAX	North America CAT1 variant – AT&T
LE910C1-ST	North America CAT1 variant – T Mobile

Module Name	Description
LE910C1-SV	North America CAT1 variant – Verizon
LE910C1-SVX	North America CAT1 variant – Verizon
LE910C1-LA	Latin America CAT1 variant
LE910C4-LA	Latin America CAT4 variant
LE910C4-CN	China CAT4 variant
LE910CX-WWX	World Wide CATX variant

The features described by the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table.

NOTE:
Information – 'X' means ThreadX OS in LE910C1-EUX, LE910C1-SAX, LE910C1-SVX and LE910CX-WWX. The other models which don't have 'X' letter are Linux OS.

CONTENTS

TABLE OF FIGURES

1. Introduction

1.1. Scope

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit's modules families shown in the Applicability Table.

1.2. Audience

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors, contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

DANGER:
Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

WARNING:
Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

NOTE:
Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

Table 2: Related Documents

Document Title	Document Number
LE910 Hardware User Guide	1vv0301089
MAX9867 Ultra-Low Power Stereo Audio Codec, MAXIM	
LE910 AT Commands Reference Guide	80421ST10585A
LE920 Hardware User Guide	1vv0301026
LE920 AT Commands Reference Guide	80407ST10116A
LE920A4 Hardware User Guide	1vv0301261
LE910Cx Hardware User Guide	1VV0301298
LE940A6/A9 Hardware User Guide	1VV0301367

1.6. Document Organization

Chapter 1: “Introduction” provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: “Overview” provides an overview of the document.

Chapter 3: “Module’s DVI (PCM)” describes the DVI port

Chapter 4: “Protocol description”

Chapter 5: “Parameters and timing characteristics”

Chapter 6: “Custom AT commands”

Chapter 7: “External codec” provides an example of interfacing with an external audio codec.

1.7. Abbreviations and Acronyms

DTE	Data Terminal Equipment
DVI	Digital Voice Interface
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
MSB	Most Significant Bit

2. Digital Voice Interface Use

Before dealing with the configuration and technical aspects of the Telit' Digital Voice Interface (DVI) it is useful to illustrate briefly where and how this interface can be used, refer to Figure 1.

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit's module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The other way round the voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.
The DVI uses the PCM or I2S interface as part of the audio front end.

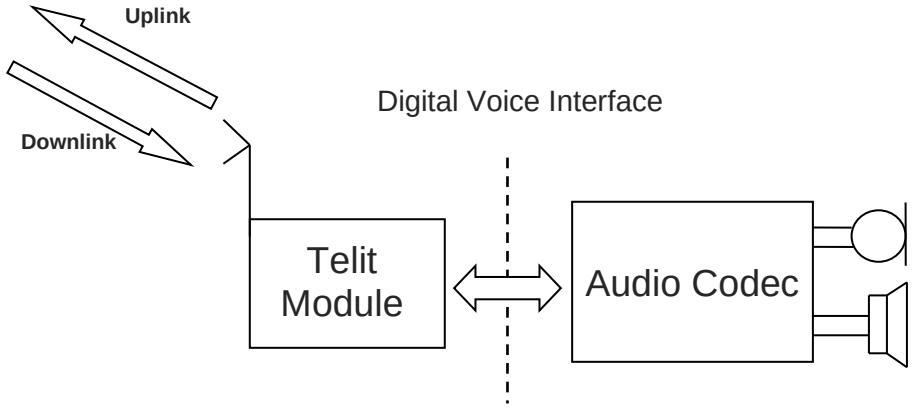

Figure 1 Example of Digital Voice Interface Use

NOTE:
LE910C1-EUX, LE910C1-SAX, LE910C1-SVX and LE910CX-WWX
Supported I2S standard only.
PCM not supported.

2.1. DVI Introduction

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.
It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.
PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8 KHz that means 125 µSec between samples) is required.

The physical DVI interface provided by the Telit's modules is based on the I2S Bus. An overview of the standard I2S Bus is described in chapter 5.1. Table. 1 summarizes the DVI signals and a short description for each one of them: refer to documents [1] and [4] to have information on electrical characteristics and signals pin-out in accordance with the used module.

DVI Signal	DVI Signal name	Description
Clock	DVI_CLK	Data Clock
Word Alignment	DVI_WAO	Frame Synchronism
serial audio data input	DVI_RX	Received Data
serial audio data output	DVI_TX	Transmitted Data

Table. 1: DVI Signals

The LE910Cx Linux OS variants support both MASTER and SLAVE Mode. LE910C1-EUX,LE910C1-SAX,LE910C1-SVX,LE910CX-WWX and other models support MASTER Molde only.
The figures below show the configuration of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself.

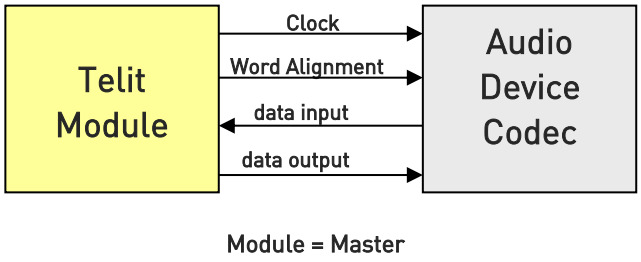

Figure 2 DVI signals

DVI Configurations

The command AT#ADSPC is usable to configure the DSP profile according to the device connected to Codec.
LE910C1-EUX,LE910C1-SAX,LE910C1-SVX and LE910CX-WWX does not support AT#ADSPC.

#ADSPC - Audio DSP Configuration	
AT#ADSPC=<n> [,<ecns mode>]	Set command switches the DSP profile audio path depending on parameter <**n**> Parameter: **<n>** - DSP profile configuration 0. Automatic (factory default) 1. Hands Free 2. Headset 3. Handset 4. Speaker phone Bluetooth 5. TTY 6. USB **< ecns mode >** 0. Disables ECNS mode (default) 1. Enables ECNS. **Note:** • On Automatic mode: Digital: handset Analog: according to #**CAP** • This command influence on the #**CAP**/ #**SRP**. • On Active/MT/MO Voice Call return Error. • When #**TTY** command enabled, SET #**ADSPC** command return Error. • The <**n**> = 5 "TTY" only configured DSP profile to "Full TTY" mode, to enable TTY mode and another TTY mode using by #**TTY** command. • The <**n**> = 6 is only supported by "Disable ECNS mode"
AT#ADSPC?	Read command reports the active DSP profile configuration in the format: For TTY profile: #ADSPC: <n> For Another DSP profile: #ADSPC: <n>, < ecns mode >.
AT#ADSPC=?	Test command reports the supported values for the parameter <n>.

The command AT#DVICFG is usable to configure the DVI interface.
LE910C1-EUX,LE910C1-SAX,LE910C1-SVX and LE910CX-WWX does not support AT#DVICFG.
Its syntax is the following:

#DVICFG – DVI CONFIGURATION	
AT#DVICFG=[<clock>[,<decoder pad>[,<decoder format>[, <encoder pad>[,<encoder format>]]]]]	Set command sets the DVI configuration Parameter: <**clock**>: Clock speed for master mode 0 : normal mode(factory default) 1 : high speed mode <**decoder pad**>: PCM padding enable in decoder path 0 : disable 1 : enable(factory default) <**decoder format**>: PCM format in decoder path 0 : u-Law 1 : A-Law 2 : linear(factory default) <**encoder pad**>: PCM padding enable in encoder path 0 : disable 1 : enable(factory default) <**encoder format**>: PCM format in encoder path 0 : u-Law 1 : A-Law 2 : linear(factory default) **Note**: • #**DVICFG** parameters are saved in the extended profile. • #**DVICFG** return Error, when #DVICLK enabled. • LE910x, LE920x supports only the first parameter <**clock**> Normal mode (factory default) = 2048KHz with sample rate 8k. High speed mode = 4096 KHz with sample rate 16k. • Another parameters (<**decoder pad**>,<**decoder format**>,<**encoder pad**>,<**encoder format**>)have no effect and are included only for backward compatibility. • The command work only for PCM mode(#**DVIEXT**=0) • #**DVICFG** return Error, when I2S mode(#**DVIEXT**=1)
AT#DVICFG=?	Test command returns the supported range of values of parameter <**clock**>, <**decoder pad**>,<**decoder format**>,<**encoder pad**>,<**encoder format**>.

The AT#DVI command enables/disables the DVI interface.
Its syntax is the following:

#DVI - Digital Voiceband Interface	
AT#DVI=<mode> [,<dviport>, <clockmode>]	Set command enables/disables the Digital Voiceband Interface. **Parameters:** <**mode**> - enables/disables the DVI. 0 – DVI disabled; (factory default) 1 – DVI enabled; <**dviport**> 2 - DVI port 2 (factory default) <**clockmode**> 0 - DVI slave 1 - DVI master (factory default) 2 - DVI master, clock always on **Note:** • **#DVI** parameters are saved in the extended profile. • <**clockmode**> 2 is not saved in the extended profile. Only <**clockmode**> 0 or 1 can be saved in the extended profile. • #**DVI** parameters are not saved in the extended profile by LE910C1-EUX /SAX/SVX and LE910Cx-WWX product. • On **<mode>** 0 supported by "DVI master" only. • When the <**clockmode**> 2, If change the <**clockmode**> 2 to <**clockmode**> 0 or 1 the device will reboot for clock off. • #**DVICFG** and #**DVICLK** return Error, when <**clockmode**> 2. If you want to set the DVI clock in **<clockmode>** 2, Please set **<clockmode>** 2 after set the DVI clock in **<clockmode>** 0 or 1. If you want to set the DVI clock in <**clockmode**> 2, Please set <**clockmode**> 2 after set the DVI clock in <**clockmode**> 0 or 1. • It impact power consumption if using <**clockmode**> 2. • The **<dviport>** parameter have no effect and is included only for backward compatibility. • On Active/MT/MO Voice Call return Error. • <**clockmode**> 0 and 2 are not supported by LE910C1-EUX/SAX/SVX and LE910Cx-WWX product. • LE910C1-EUX /SAX/SVX and LE910Cx-WWX product only supports I2S interface.
AT#DVI?	Read command reports last setting, in the format: **#DVI**: <**mode**>,<**dviport**>,<**clockmode**>
AT#DVI=?	**Test command reports the range of supported values for parameters <mode>,<dviport> and <clockmode>**
Example	**AT#DVI**=1,2,1 OK DVI activated for audio. DVI is configured as master providing on DVI Port #2

The LE910x Linux OS modules have the following possible configurations:

Normal mode (factory default)
- Master Mode
- 8KHz
- 16 bits
- 2.048MHz clock

High Speed mode
- Master Mode
- 16KHz
- 16 bits
- 4.096MHz clock

The LE920x Linux OS modules have the following possible configurations:

Normal mode (factory default)
- Master Mode
- 8KHz
- 16 bits
- 2.048MHz clock

High Speed mode
- Master Mode
- 16KHz
- 16 bits
- 4.096MHz clock

#DVICLK - Digital Voiceband Interface Extension	
AT#DVICLK=<clock>[,<samplerate>]	Set command configures and activates the DVICLK clock signal and the Digital Voiceband Interface Parameters: **<clock>** 0 – Disable (factory default) 128 – DVI Clock activated at 128KHz 256 – DVI Clock activated at 256KHz 512 – DVI Clock activated at 512KHz 1024 – DVI Clock activated at 1024KHz 2048 – DVI Clock activated at 2048KHz 4096 – DVI Clock activated at 4096KHz **<samplerate>** 0 - audio scheduler sample rate 8KHz (factory default) 1 - audio scheduler sample rate 16KHz Note : • On Active/MT/MO Voice Call return Error. • Clock 4096KHz don't supported with Sample Rate 8KHz • #**DVICFG** return Error, when <clock> enabled.

#DVICLK - Digital Voiceband Interface Extension	
	• On Clock value zero (0) the clock rate and sample rate taken from #**DVICFG** <**clock**> value. • This parameter is saved in NVM issuing AT&W command. • The command work only for PCM mode (#**DVIEXT**=0) • #**DVICLK** return Error, when I2S mode (#**DVIEXT**=1) • #**DVICLK** return Error, when clock always on mode (#DVI=1,2,2) • For LE910C1-EUX /SAX/SVX and LE910Cx-WWX product: • Clock 256KHz supports only Sample Rate 8KHz. • Clock 512KHz supports only Sample Rate 16KHz. • Both <**clock**> and <**samplerate**> should be entered. #**DVICLK** return Error, if only <**clock**> is enter. • Factory default is <**clock**> 256 and <**samplerate**> 0(8KHz). • Not support #**DVICFG**. • Not supports <**clock**> 0, <**clock**> 128, <**clock**> 1024, <**clock**> 2048, <**clock**> 4096. • This parameter is not save in NVM.
AT#DVICLK?	Read command reports last setting, in the format: **#DVICLK:< clock > ,<samplerate>**
AT#DVICLK =?	Test command returns the range of supported values for all the sub parameters.

The command AT#DVIEXT is usable to configure the Extended DVI interface.
LE910C1-EUX,LE910C1-SAX,LE910C1-SVX and LE910CX-WWX does not support AT#DVIEXT.
Its syntax is the following:

#DVIEXT – Extended Digital Voiceband Interface	
AT#DVIEXT=<config>[,<samplerate>[,<samplewidth>[,<audiomode>[,<edge>]]]]	Set command configures the Digital Voiceband Interface. **Parameters**: <**config**> 0 – PCM Mode (factory default) 1 – I2S Mode <**samplerate**> 0 – audio scheduler sample rate 8KHz (factory default) 1 – audio scheduler sample rate 16KHz 2 – audio scheduler sample rate 48KHz <**samplewidth**> 0 – samplewidth has no effect is included only for backward compatibility. <**audiomode**> 0 – audiomode has no effect is included only for backward compatibility. <**edge**> 0 – edge has no effect is included only for backward compatibility.

#DVIEXT – Extended Digital Voiceband Interface	
	Note: Sample width has to be only in I2S Mode. **Note**: Manual reboot is required after changing. **Note**: The setting is saved in system. **Note**: Supported samplewidth is 16bit only.
AT#DVIEXT?	Read command reports last setting, in the format: **#DVIEXT: <config>,<samplerate>,< samplewidth>,<audiomode>, <edge>**
AT#DVIEXT=?	Test command reports the supported range of values for the parameters <**config**>,<**samplerate**>,< **samplewidth**>, <**audiomode**>,<**edge**>

3. Timing Characteristics

Parameter	Description	Min	Typical	Max	Units
t(sync)	PCM_SYNC cycle time	-	125	-	us
t(syncha)	PCM_SYNC asserted time	-	488	-	ns
t(syncd)	PCM_SYNC de-asserted time	-	124.5	-	us
t(clk)	PCM_CLOCK cycle time	-	488	-	ns
t(clkh)	PCM_CLOCK high time	-	244	-	ns
t(clkl)	PCM_CLOCK low time	-	244	-	ns
t(sync_offset)	PCM_SYNC offset time to PCM_CLOCK falling	-	122	-	ns
t(sudin)	PCM_RX setup time to PCM_CLOCK falling	60	-	-	ns
t(hdin)	PCM_RX hold time after PCM_CLOCK falling	60	-	-	ns
t(pdout)	Delay from PCM_CLOCK rising to PCM_TX valid	-	-	60	ns
t(zdout)	Delay from PCM_CLOCK falling to PCM_TX HIGH-Z	-	-	60	ns

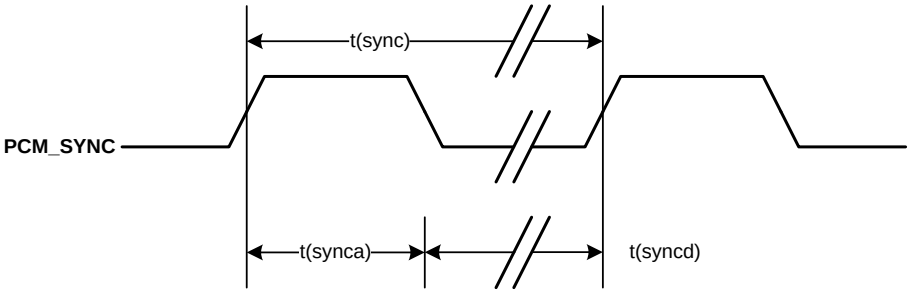

Figure 3 Primary PCM_SYNC timing (Short sync, 2048kHz clock)

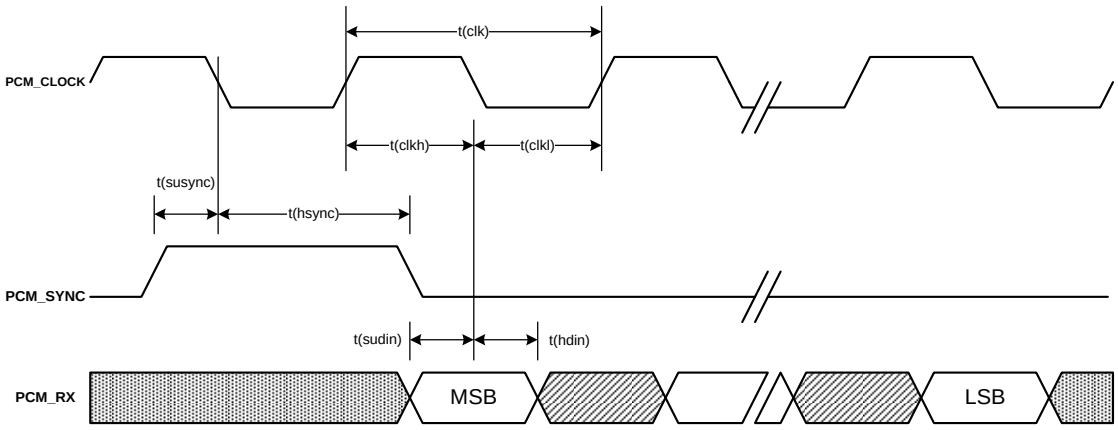

Figure 4 External codec to LE910 timing

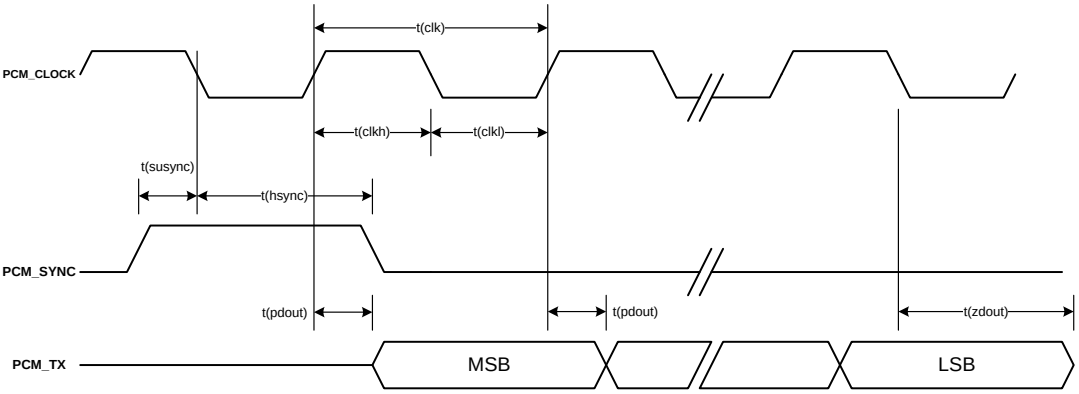

Figure 5 LE910 to External codec timing

4. DVI Setting

The next chapters show how to configure an external codec connected to the Module.
All the following setting examples are performed using the hardware configuration shown in Figure 6.

I2C bus is used to configure the MAX9867 Codec1 [2].
The DVI bus provides the voice connection between the two devices.

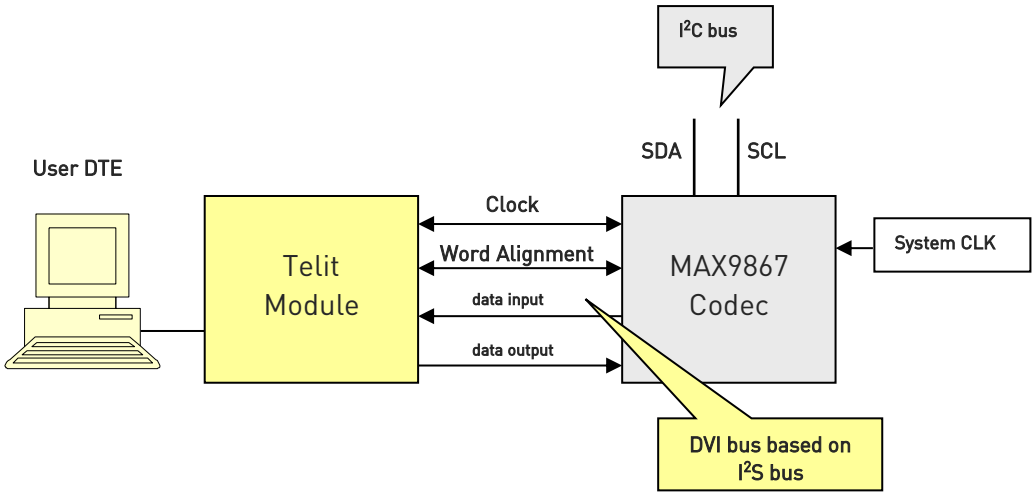

Figure 6 Telit Module/Codec Connections

NOTE: The CODEC Example is applicable only to the High Speed mode
- Master Mode
- 16KHz
- 16 bits
- 4.096 MHz clock

NOTE: Chapter "4. DVI Setting" is an example only for the PCM interface of the Linux OS module.

[1] The following examples use the MAX9867 Codec, see chapter 5.4 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the Telit's modules.

The module has the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the audio channel.

The following part is showing the commands necessary to set the DVI and the codec

Configure the DVI

DVI bus

AT#DVICFG=1,1,2,1,2
OK

1	High Speed Mode
1	decoder pad enabled
2	decoder format Linear
1	encoder pad enabled
2	encoder format Linear

Set the Module in Master Mode

DVI bus

AT#DVI=1,2,1
OK

1	enable DVI interface
2	use DVI port 2 (mandatory)
1	set the module as Master (factory setting)

Configure the codec in Slave, Burst(PCM) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>0010900004000000300000000B0B3414C00000

OK

X	GPIO number used as SDA, refer to [3]
Y	GPIO number used as SCL, refer to [3]
30	Device address on I^2C, refer to [2]
4	Register address from which start the writing, refer to [2]
19	number of bytes to write

>00101000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X	GPIO number used as SDA, refer to [3]
Y	GPIO number used as SCL, refer to [3]
30	Device address on I^2C, refer to [2]
17	Register address where write data, refer to [2]
1	number of bytes to write

>8A, refer to [2]

Here are the lists of AT commands used to set the module in Slave Burst (PCM) Mode, and configure the codec in accordance with the current module setting. After each command is described the used parameters values meaning.

Configure the module in Slave Burst(PCM) Mode

DVI bus

AT#DVI=1,2,0
OK

1 enable DVI interface
2 use DVI port 2 (mandatory)
0 set the module as Slave

Configure the DVI clock

DVI bus

AT#DVICLK=<clock>,<samplerate>
OK

<**clock**> PCM clock frequency which is driven from the external codec (in KHz)
<**samplerate** > PCM Frame sync rate which is driven from the external codec (“0” => 8KHz, “1” => 16KHz)

Configure the codec in Master Burst (PCM) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>00101000A40A330000330C0C09092424400060

OK

X GPIO number used as SDA]
Y GPIO number used as SCL
30 Device address on I2C
4 Register address from which start the writing
19 number of bytes to write
>00101000…..refer to MAX9867 document

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I2C
17 Register address where write data
1 number of bytes to write
> 8A refer to MAX9867 document

Slave mode example for Configure the MAX9867 Codec & Module

Option 1 :
Codec clock 1024 KHz
Sample rate 16KHz

AT#DVI=1,2,0
OK
AT#DVICLK=1024,1
OK

AT#I2CWR=2,3,30,4,19
> 00102000A401000300000000017173414C00000
OK

AT#I2CWR=2,3,30,17,1
> 8a
OK

Option 2 :
Codec clock 512KHz
Sample rate 8KHz

AT#DVI=1,2,0
OK
AT#DVICLK=512,0
OK

AT#I2CWR=2,3,30,4,19
> 00101000A401000030000000017173414C00000
OK

AT#I2CWR=2,3,30,17,1
> 8a
OK

The CODEC configuration is described in the following table (refer to the MAX9867 datasheet for the details):

Register address	Register Name	Value (Hex)	Value (Bin)	Description
0x04	Interrupt Enable	0	0	Disabled
0x05	System Clock	10	10000	MCLK is between 10MHz and 20MHz (12.288MHz in our example); Frequency: Normal mode The frequency of LRCLK is set by the NI divider bits. Due to the fact the COD is Slave, it expects an LRCLK as specified by the divide ratio
0x06	Audio Clock High	20		NI=0x2000 --> 16KHz
0x07	Audio Clock Low	0	0	
0x08	Interface mode 1a	4	100	MAS=0 : The MAX9867 operates in slave mode with LRCLK and BCLK configured as inputs. WCI ignored because TDM=1 BCI=0 : SDIN is latched into the part on the rising edge of BCLK. SDOUT transitions after the rising edge of BCLK as determined by SDODLY*. DLY ignored because TDM=1 HIZOFF=0 : SDOUT goes to a high-impedance state after all data bits have been transferred out of the MAX9867, allowing SDOUT to be shared by other devices. TDM=1 : LRCLK is a framing pulse that transitions polarity to indicate the start of a frame of audio data consisting of multiple channels. When operating in TDM mode, the left channel is output immediately following the frame sync pulse. If rightchannel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data.
0x09	Interface mode 1b	0	0	LVOLFIX=0 : DMONO=0 : Stereo data input on SDIN is processed separately. BSEL=0 : No effect becasue in Slave Mode
0x0A	Codec Filters	33	110011	MODE=0 : 0 = IIR Voice Filters AVFLT = 0x3 : Filter Eliptical, Sample Rate 8KHz, HighPass Corner Freq 256Hz, 217Hz Notch active. DVFLT= 0x3 : Filter Eliptical, Sample Rate 8KHz, HighPass Corner Freq 256Hz, 217Hz Notch Active.
0x0B	DAC Gain/Sidetone	0	0	DSTS=0 : 00 = No sidetone is selected. DVST=0 : Disabled
0x0C	DAC Level	0	0	DACM=0 : NO Mute DACG=0 : 0dB DACA=0 : 0dB Gain
0x0D	ADC Level	33	110011	AVL=0x3 : 0dB Gain AVR=0x3 : 0dB Gain
0x0E	Left Line Input Level	0C	1100	LILM=0 : Line input is connected to the headphone amplifiers. LIRM=0 : Line input is connected to the headphone amplifiers.
0x0F	Right Line Input Level	0C	1100	LIGL = 0xC : 0dB Gain LIGR = 0xC : 0dB Gain
0x10	Left Volume Control	9	1001	VOLLM=0 : Audio playback is unmuted. VOLL=0x9 : 0dB Gain

0x11	Rigth Volume Control	9	1001	VOLRM=0 : Audio playback is unmuted. VOLR= 0x9 : 0dB Gain
0x12	Left Mic Gain	24	100100	PALEN=0x01 : PreAmplifier Gain=0dB PGAML=0x4 : Gain =+16dB
0x13	Rigth Mic Gain	24	100100	PALEN=0x01 : PreAmplifier Gain=0dB PGAML=0x4 : Gain =+16dB
0x14	ADC Input	40	1000000	MXNL= 01 = Left analog microphone MXNR= 00 = No Input selected AUXCAP=0 : Update AUX with the voltage at JACKSNS/AUX. AUXGAIN=0 : Normal operation AUXCAL=0 : Normal operation AUXEN=0 : Use JACKSNS/AUX for jack detection.
0x15	Microphone	0	0	MICCLK=0 : PCLK/8 DIGMICL=0 and DIGMICR=0 : Left ADC input= ADC input mixer, Right ADC Input=ADC input mixer.
0x16	Mode	60	1100000	DSLEW=0 : Digital volume changes are slewed over 10ms. VSEN*=1 : Volume changes occur in one step. ZDEN*=1 : Line-input volume changes occur immediately. JDETEN=0 : Enables pullups on LOUTP and JACKSNS/AUX to detect jack insertion. LSNS and JKSNS are valid. LOUTP detection is only valid in differential and capacitorless output modes. HPMODE=0 : Stereo differential (clickless)
0x17	System Shutdown	8A	10001010	SHDN*=1 : Places the device in low-power shutdown mode. LNLEN=0 : Left-Line Input disabled LNREN=0 : Rigth-Line Input disabled DALEN=1 : Enables the left DAC and automatically enables the left and right headphone amplifiers. DAREN=0 : Right DAC disabled ADLEN=1 : Left ADC Enabled ADREN=0 : Right ADC disabled

5. Annex

5.1. I²S Overview

This chapter provides a short description of the standard I2S bus. This standard suitably modified is used by the DVI interface implemented on the Telit's modules.

The standard I2S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to Figure 7 the I2S design handles audio data separately from clock signals. On an I2S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a Codec, the Codec is typically the master so that it has precise control over the I2S bus clock.

An I2S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I2S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

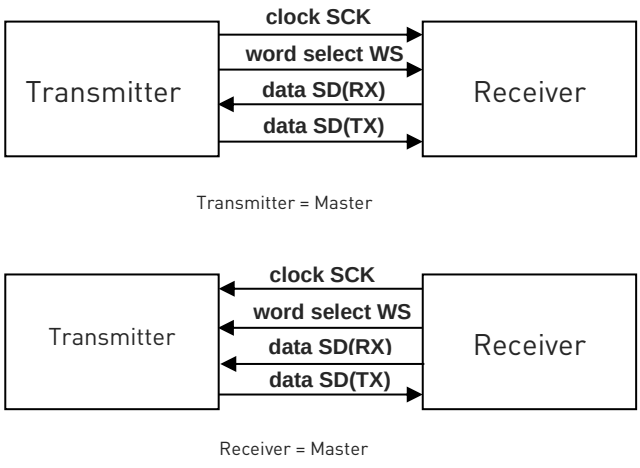

Figure 7 I2S bus configurations

5.2. I²S Timing Characteristics

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
	Frequency		-	-	12.288	MHz
T	Clock period		81.380	-	-	ns
t(HC)	Clock high		0.45 * T	-	0.55 * T	ns
t(LC)	Clock low		0.45 * T	-	0.55 * T	ns
t(sr)	SD and WS input setup time		16.276	-	-	ns
t(hr)	SD and WS input hold time		0		-	ns
t(dtr)	SD and WS output delay		-	-	65.100	ns
t(htr)	SD and WS output hold time		0	-	-	ns
Using external SCK						
	Frequency		-	-	12.288	MHz
T	Clock period		81.380	-	-	ns
t(HC)	Clock high		0.45 * T	-	0.55 * T	ns
t(LC)	Clock low		0.45 * T	-	0.55 * T	ns
t(sr)	SD and WS input setup time		16.276	-	-	ns
t(hr)	SD and WS input hold time		0		-	ns
t(dtr)	SD and WS output delay		-	-	65.100	ns
t(htr)	SD and WS output hold time		0	-	-	ns

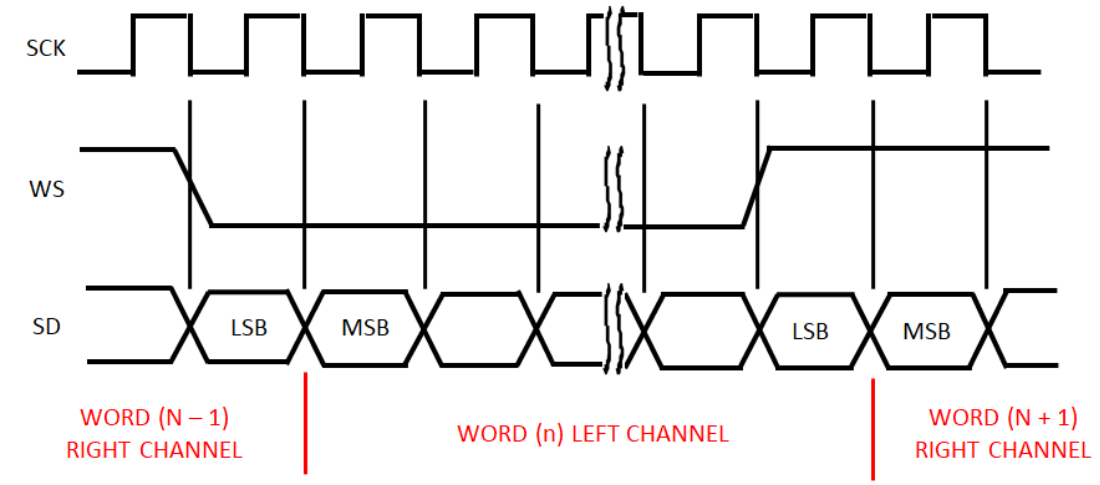

Figure 8 High-level I2S timing

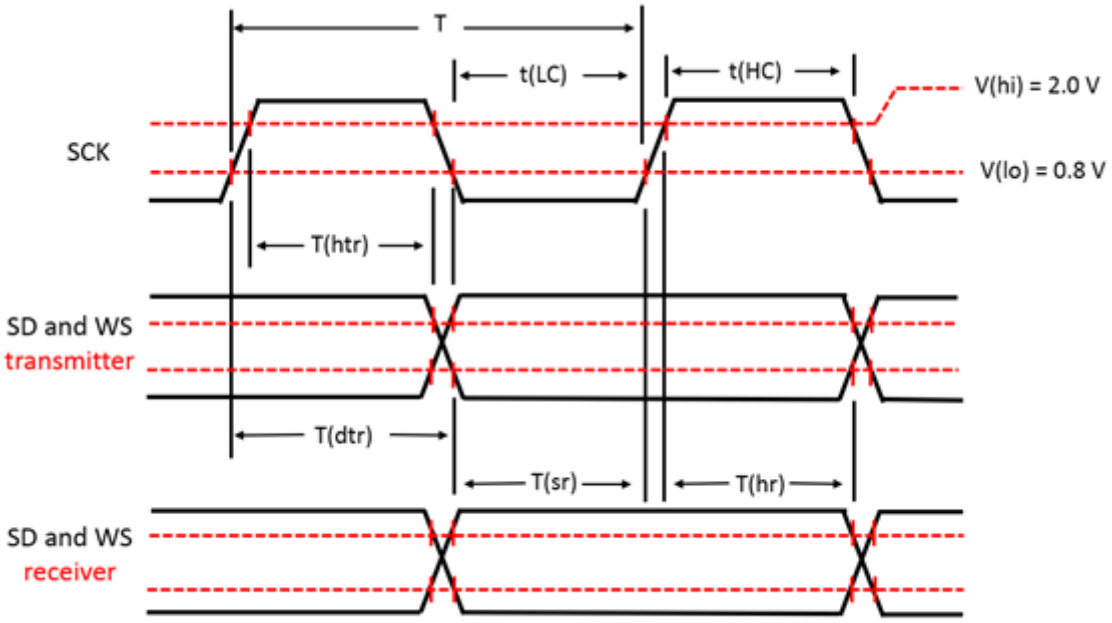

Figure 9 I2S timing details Tx & Rx

5.3. LE910Cx I2S characteristics

- Sample rate: 8KHz, 16KHz, 48KHz
- Sample width: 16bit
- Supported I2S standard only - Phillips I2S Bus Specifications revised June 5, 1996

5.4. Schematic

A schematic example of an interface between the Telit's modules and the MAX9867 CODEC could be the following:

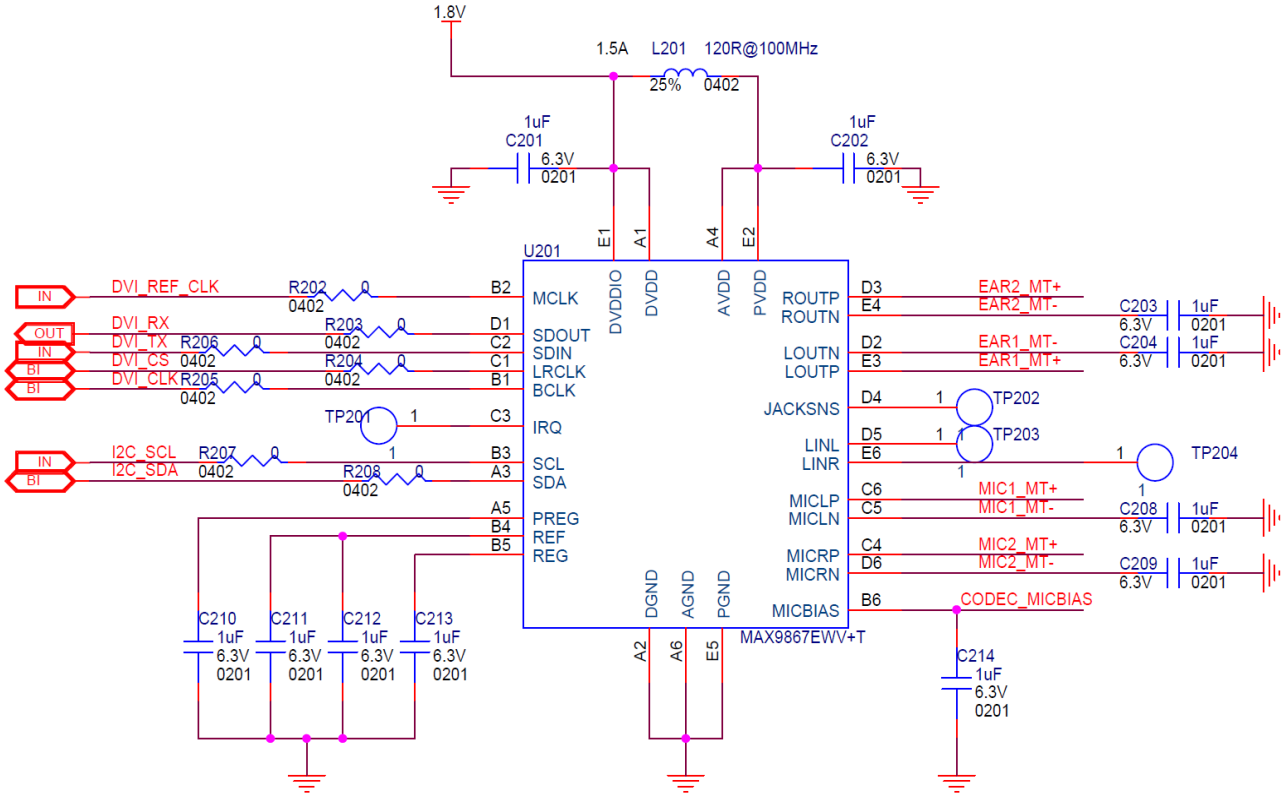

Figure 10 Schematic for Reference Design

6. Revision History

REV	DATE	CHANGES
0	2014-03-31	First issue
1	2014-08-08	Updated supported modes
2	2014-08-22	Updated supported modes Added note on CODEC example applicability
3	2014-11-09	Add LE920 support Updated DVI command setting
4	2015-09-24	Updated supported modes Updated supported LE910, LE920 models
5	2017-03-30	Updated supported LE910Cx, LE920A4 models Updated documents template Cosmeics updates of tables and drawings
6	2019-06-24	Added LE910Cx variants and AT commands related
7	2019-06-28	Updated DVI command setting
8	2021-01-11	Added I2S Timing Characteristics
9	2021-01-27	Updated I2S Overview Added I2S LE910Cx I2S characteristics Added LE910C1-EUX, LE910C1-SAX, LE910C1-SVX and LE910CX-WWX variant

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